What is claimed is:

1. A semiconductor, comprising

a gate electrode and a gate oxide layer on a semiconductor substrate;

spacers formed on sides of the layer;

a first conductive type source/drain region formed at edge of the spacers in the semiconductor substrate;

a second conductive type punch stop layer formed in a region between the first conductive type source/drain region in the semiconductor substrate;

a first conductive type source/drain extension region occupying a extended region from the first conductive type source/drain region to the both edges of the gate electrode; and

a first conductive type lightly doped drain (LDD) region being adjoined to the source/drain region and surrounding the source/drain extension region, wherein the junction depth of the first conductive type LDD region is constrained by the punch stop layer.

2. The semiconductor as recited in claim 1, wherein the first conductive type LDD region has lower impurity concentration comparing to the first conductive type source/drain region and the first conductive type source/drain extension region.

3. The semiconductor as recited in claim 1, the thickness of the first conductive type source/drain extension region is thinner than the first conductive type source/drain region and the depth of the first conductive type LDD region is deeper than the first conductive type source/drain extension region and shallow than the source/drain region.

4. The semiconductor as recited in claim 1, the first conductive type LDD region has at least duplicate structure that surrounds the first conductive type source/drain extension region.

5. The semiconductor as recited in claim 1, further comprising:

a second conductive type field stop layer, which is deeper than the second conductive type punch stop layer; and

a second conductive type well region, which is deeper than the first conductive type field stop layer.

6. The semiconductor as recited in claim 1, wherein the first conductive type source/drain extension region and the first conductive type LDD region are an conductive type impurity doping layer having different extension rate and the extension rate of the impurity in the first conductive type LDD region is faster.

7. The semiconductor as recited in claim 6, wherein

arsenic is implanted to the first conductive type source/drain extension region and phosphorous is implanted to the first conductive type LDD region.

8. A semiconductor device, comprising:

a semiconductor substrate having a nMOS region and a pMOS region;

a gate electrode and a gate oxide layer formed on each of the nMOS region and the pMOS region;

spacers contacted to sides of the layer;

a p-type source/drain region formed in the pMOS region by lining up at edges of the spacers;

a n-type source/drain region formed in the nMOS region by lining up at edges of the spacers;

a first punch stop layer formed by overlapped on bottom of the p-type source/drain region;

a second punch stop layer formed by contacting to one side of the p-type source/drain region and on the bottom of the spacers;

a third punch stop layer formed by contacting to one side of the n-type source/drain region;

a source/drain extension region formed by contacting to one side of the n-type source/drain region and on bottom of the spacers; and

a lightly doped drain (LDD) region surrounding the source/drain extension region.

9. The semiconductor as recited in claim 8, wherein the LDD region has a multiple layer structure by a number of times doped with identical impurity.

10. The semiconductor as recited in claim 8, wherein the source/drain extension region and the LDD region are an conductive type impurity doping layer having different extension rate and the extension rate of the impurity in the first conductive type LDD region is faster.

11. The semiconductor as recited in claim 10, wherein the source/drain region is a doping layer of arsenic and the LDD region is a doping layer of phosphorous.

12. The semiconductor as recited in claim 8, wherein an impurity concentration of the LDD region is in low comparing to the n-type source/drain region and the source/drain extension region.

13. The semiconductor as recited in claim 8, wherein the first punch stop layer is a doping layer of an arsenic and the second punch stop layer is a doping layer of phosphorous.

14. A method for fabricating a CMOS transistor, comprising:

a) forming a n-type well region in a semiconductor substrate;

b) forming a first n-type punch stop layer in the n-type well;

c) forming a p-type well region in the n-type well region;

d) concurrently forming a first n-type LDD region in the p-type well region and a second n-type punch stop layer in the n-type well region by ion-implanting an impurity to the gate electrode as a mask;

e) forming a n-type source/drain extension region having higher concentration of the impurity than the first LDD region in the first LDD regions;

f) forming a second n-type LDD region, which surrounds the n-type source/drain extension region;

g) forming a spacer at a side of the gate electrode;

h) forming p-type source/drain region contacting to the first punch stop layer and the second punch stop layer; and

i) forming a n-type source/drain region contacting to the source/drain extension region and the first and second LLD region.

15. The method as recited in claim 14, wherein a depth of the second LDD region is same or deeper than the first LDD region.

16. The method as recited in claim 14, further comprising j) forming a first p-type punch stop layer in bottom of the first LDD region after forming the first LDD

region.

17. The method as recited in claim 14, wherein an impurity concentrations of the first and second LDD regions are comparatively lower than the source/drain extension region.

18. The method as recited in claim 14, wherein the first and second LDD regions are formed by ion-implanting a first n-type impurity and the source/drain extension region is formed by ion-implanting a second n-type impurity, wherein the first n-type impurity is spread faster than the second n-type impurity.

19. The method as recited in claim 14, wherein the first n-type impurity is a phosphorous and the second n-type impurity is an arsenic.

20. The method as recited in claim 14, wherein the first punch stop layer is formed by ion-implanting an arsenic or an antimony.

21. The method as recited in claim 14, wherein the step e) ion implants a phosphorous to an entire surface.